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Date: 08/10/2005

Cover Sheet + 5 Pages

Message:

RE: Patent Application No.: 09/715,772
Filed: 11/17/2000
Inventor: Dennis
Docket No.: NC 84,781
Response to Final Rejection – 5 pages

PATENT APPLICATION
Docket No.: NC 84,781

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of: Dennis
Serial No.: 09/715,772
Filed: 11/17/2000
For: MULTI-THREAD PERIPHERAL PROCESSING USING DEDICATED PERIPHERAL BUS
Examiner: King, Justin
Art Group Unit: 2181

Honorable Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

August 10, 2005

RESPONSE TO FINAL REJECTION

Sir:

In response to the Office action of 07/19/2005, setting a three month shortened statutory period of response, please consider the following remarks.

Claims 1-41 are pending in the application. No claims are presently allowed.

Claim Rejections – 35 U.S.C. § 102

Claims 1-12, 14-25, 27-38, and 41 have been rejected under 35 U.S.C § 102(b) as allegedly anticipated by Motomura (US 5,815,727).

Claim 1 recites an apparatus comprising: a peripheral bus coupled to a peripheral unit and a processing slice coupled to the peripheral bus. The peripheral bus transfers peripheral information including a command message specifying a peripheral operation. The processing slice executes a plurality of threads comprising instructions. The threads include a first thread sending the command message to the peripheral unit. The processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each

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thread. The processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

Motomura discloses a multi-thread parallel processor system having a plurality of processors and an ordered multithread executing system (Fig. 1). The ordered multithread executing system determines which thread will execute on each processor.

In order to make a *prima facie* case of anticipation, the reference must disclose each limitation of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053, 814 F.2d 628, 631 (Fed. Cir. 1987); MPEP 2131. Among other deficiencies, the reference does not disclose the limitation in claim 1 that the functional unit performs a register operation specified in the instructions dispatched from each thread.

As previously amended, claim 1 clarifies that instructions may be dispatched from each thread to the functional unit. This avoids an interpretation that functional unit is capable of executing such instructions, but does not actually do so. In the present claim, instructions may be dispatched from each thread to the functional unit. Thus the functional unit is not dedicated to a single thread.

In response to the above paragraph, the Examiner stated that the amendment to claim 1 does not avoid an interpretation of the functional unit being capable of executing instructions dispatched from each thread. (Office Action of 07/19/2005, page 13, lines 5-10.) However, Applicant's interpretation of present claim 1 is that it requires that the functional unit executes instructions dispatched from each thread. The amendment was made in response to Applicant's understanding of the Examiner's explanation that all of the processors of Motomura use the same instruction set, and so each processor could perform an operation from each thread. (Paper 17, page 13, lines 3-10.) However, although a first processor in Motomura may have the capability to perform an instruction from a thread executing on a second processor, Motomura's system does not dispatch the instruction to the first processor and is not configured to do so. The instruction is executed only by the second processor, which is the processor to which the thread is assigned. Thus in Motomura, a processor is allegedly capable of executing instructions from each thread, but does not actually do so. In contrast, claim 1 recites that instructions from each thread are dispatched to the functional unit. The functional unit is capable of executing instructions from each thread, and does actually do so.

The Examiner stated that Fig. 1, structure 100 of Motomura discloses Applicant's

processing slice and that Motomura's processor discloses Applicant's functional unit (Office Action of 07/19/2005, p. 2, lines 1-3). Although the system of Motomura as a whole is capable of simultaneous execution of multiple threads, there is no sharing of functional units among threads. Motomura discloses that each processor can execute only one thread at a time, in that the thread must go into a waiting or completed state before another thread is assigned to the processor (col. 8, lines 40-51). Further, there are no connections disclosed between processors. Each processor can communicate only with the ordered multithread execution system and the memory device (Fig. 1). The result of this configuration is that each processor is dedicated only to the one thread that can execute on that processor at a time. An idle processor cannot be allocated to a thread executing on another processor. In the present application, it is specifically recited in the claims that the functional unit can perform a register operation specified in the instructions dispatched from *each* of the threads, which are simultaneously executing. Motomura lacks this capability because each processor can perform operations dispatched from only *one* thread.

The Examiner stated that Motomura discloses forking and requirement of other threads during execution, which is sharing functional units among threads (Office Action of 07/19/2005, p. 13, lines 16-19). In the forking situation, the forking thread is executing on one processor and the forked thread is executing on another processor. Thus, each processor is executing only one thread, and no instructions from a thread are dispatched to the other processor. In the case of a processor requesting another thread, the first thread is placed in a waiting state (col. 8, lines 40-41). Thus, the processor is only executing instructions from the active thread, and no instructions are dispatched to the processor from the waiting thread. Thus, the processor is dedicated to the active thread and is not shared among threads.

Claims 14, 27, and 41 also contain the limitation regarding the functional unit and are asserted to differ from the reference in the same manner as claim 1. Claims 2-12, 15-25, and 28-38 depend from and contain all the limitations of claims 1, 14, or 27 and are also asserted to differ from the reference in the same manner as claim 1.

Claim Rejections – 35 U.S.C. § 103

Claims 13, 26, and 39 have been rejected under 35 U.S.C § 103(a) as allegedly unpatentable over Motomura in view of Hiraoka et al. (US 5,418,917).

Hiraoka discloses a method and apparatus for controlling a conditional branch instruction in a pipeline type data processing apparatus.

In order to make a *prima facie* case of obviousness, each claim limitation must be disclosed in the references (MPEP 2143.03). As in Motomura, Hiraoka does not disclose the limitation in claims 1 (13 dependent thereon), 14 (26 dependent thereon), and 27 (39 dependent thereon) regarding the functional unit. As neither of the references discloses the functional unit, a *prima facie* case of obviousness has not been made.

Claim 40 has been rejected under 35 U.S.C § 103(a) as allegedly unpatentable over Motomura in view of Dove et al. (US 5,938,765).

Claim 40 recites a processing system comprising a plurality of multi-thread processors, a plurality of peripheral units, and a peripheral bus. Each processor comprises a plurality of processing slices including a functional unit.

Dove discloses an apparatus and method for initializing a shared-memory, multimode multiprocessor computer system. As in Motomura, Dove does not disclose the limitation in claim 40 regarding the functional unit. As neither of the references discloses the functional unit, a *prima facie* case of obviousness has not been made.

The Examiner stated that Applicant had not responded to his previous statement that the specification does not disclose a processing slice with a plurality of processing units (Office Action of 07/19/2005, p. 13, lines 16-19). The basis for the objection was a citation to Paper 13, page 3, lines 6-7, which the Examiner stated to state that the processing slice is able to dispatch instructions to any of the functional units within the processing unit. (Paper 17, page 14, lines 2-4.) However, the actual sentence from the Paper 13 is "The processing slice is able to dispatch an instruction from any currently executing thread to any of the functional units within the processing slice." (Emphasis added.)

In view of the foregoing, it is submitted that the application is now in condition for allowance.

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Respectfully submitted,

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